IN THE CLAIMS

1. (Original) A method of forming a floating gate transistor comprising:

forming laterally spaced source and drain regions to define a channel therebetween;

forming a first floating gate portion above the channel region, the first floating gate portion extending in a general horizontal direction;

forming spacers over the first floating gate portion to define an exposed region on the first floating gate portion;

forming a contact coupled to the first floating gate portion at the exposed region, the contact extending vertically above the first portion;

forming a second floating gate portion coupled to the contact, the second floating gate portion extending in a general vertical direction; and

forming a control gate adjacent to the second portion.

2. (Original) The method of claim 1, wherein forming spacers comprises forming nitride spacers.

3. (Original) The method of claim 1, wherein forming the second floating gate portion comprises forming a container-shaped portion.

4. (Original) The method of claim 3, wherein forming the control gate comprises forming the control gate substantially within a center opening of the container-shaped portion.

5. (Original) A method of forming a floating gate transistor comprising:

forming laterally spaced source and drain regions to define a channel therebetween;

forming a substantially flat floating gate portion above the channel region;

forming spacers over the flat floating gate portion to define an exposed region on the flat floating gate portion;

forming a contact coupled to the flat floating gate portion at the exposed region, the contact extending vertically above the flat floating gate portion;

forming a vertically extending floating gate container portion coupled to the contact, the floating gate container portion having interior and exterior regions; and

forming a control gate adjacent to the floating gate container portion.

6. (Original) The method of claim 5, wherein forming the control gate comprises forming the control gate inside the interior region of the floating gate container portion.

7. (Original) The method of claim 6, wherein forming the control gate further comprises forming the control gate adjacent to the exterior region of the floating gate container portion.

8. (Original) The method of claim 5, further comprising insulating the flat floating gate portion from the channel region.

9. (Original) The method of claim 5, wherein forming the flat floating gate portion, contact, and floating gate container portion comprises forming the flat floating gate portion, contact, and floating gate container portion from a polysilicon material.

10. (Original) The method of claim 9, wherein forming the floating gate container portion further comprises forming the floating gate container portion from a hemispherical grain (HSG) polysilicon material.

11. (Original) A method of forming a floating gate transistor comprising:

forming laterally spaced source and drain regions to define a channel therebetween;

forming a first layer of oxide over the channel;

forming a semiconductive first floating gate portion laterally extending over the first layer of oxide and above the channel;

forming a vertically extending semiconductive contact coupled to the first floating gate portion, wherein fabricating the contact comprises fabricating spacers over the first floating gate portion to define an exposed central region of a top surface of the first floating gate portion, wherein the contact is fabricated to couple to the first floating gate portion at the exposed central region;

forming a vertically extending semiconductive container coupled to the contact;

forming a second layer of oxide over the container; and

forming a control gate over the second layer of oxide to provide electrical coupling to the container.

12. (Original) The method of claim 11, wherein the first floating gate portion, the contact and the container are formed using a polysilicon material.

13. (Original) The method of claim 11, wherein the control gate vertically descends into a central opening of the container.

14. (Original) The method of claim 11, wherein the first oxide layer is a tunnel oxide.

15. (Original) The method of claim 11, wherein the spacers are nitride spacers.

16. (Original) A method of forming a floating gate transistor comprising:

implanting laterally spaced source and drain regions into a substrate to define a channel therebetween;

growing a layer of tunnel oxide over the substrate;

depositing a polysilicon first floating gate portion laterally extending over the tunnel oxide and positioned above the channel;

forming a polysilicon contact over the first floating gate portion, such that the contact is coupled to the first floating gate portion, wherein forming the contact comprises forming spacers over the first floating gate portion to define an exposed central region of a top surface of the first floating gate portion, wherein the contact is coupled to the first floating gate portion at the exposed central region;

forming a polysilicon vertically extending container above the contact, such that the container is coupled to the contact;

depositing a layer of oxide over the container; and

forming a polysilicon control gate over the layer of oxide, wherein the control gate vertically descends into a central opening of the container.

17. (Original) The method of claim 16 wherein the polysilicon vertically extending container comprises a hemispherical grain (HSG) polysilicon material.